DESIGN AND APPLICATION OF FPGA HARDWARE ARCHITECTURE FOR PARALLEL DATA PROCESSING

SHORT SYNOPSIS

Submitted in partial fulfillment of the requirement of the degree of

DOCTOR OF PHILOSOPHY

To

Manav Rachna International Institute of Research and Studies
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by

Scholar Name: Sudhir Dagar
Registration number: 16/PhD/046

Under the supervision of

Dr. Geeta Nijhawan
Professor, Faculty of Electronics and Communication Engineering

FACULTY OF ENGINEERING AND TECHONOLOGY

MANAV RACHNA INTERNATIONAL INSTITUTE OF RESEARCH & STUDIES

SECTOR-43, SURAJKUND –DELHI ROAD, FARIDABAD – 121001

FACULTY OF ENGINEERING AND TECHONOLOGY

Certificate

I hereby declare that the short synopsis "**DESIGN AND APPLICATION OF FPGA HARDWARE ARCHITECTURE FOR PARALLEL DATA PROCESSING**" being submitted in partial fulfillment of the requirement for the degree of Doctor of Philosophy in Electronics and Communication Engineering under faculty of Engineering and Technology of Manav Rachna International Institute of Research & Studies, Faridabad during the academic year 2016-17.

It is a bona fide record of original work carried out under the supervision of Dr. Geeta Nijhawan and has not been submitted in full or part to any other university or institute for degree or diploma. Further, it is certified that short synopsis is plagiarism free and proof has been submitted.

(Sudhir Dagar)
Registration number: 16/PhD/046

Signature of the Supervisor
Full name: Dr.Geeta Nijhawan
Designation: Professor

(Chairman, DRC)

Chairperson, CDP

ABSTRACT

Moving objects may be diagnosed by detection structures that apply computer observation as it moves in forefront of a digital photographic camera. The prime task is to obtain identification in absolute time, and to support visible evaluation, a hard drive structure in Field Programmable Gate Arrays (FPGA) might be applied for video computing focused at the identification of moving items using the Backdrop subtraction method. The principle characteristic of FPGA chip is that it's far reprogrammable and utilizes SRAM generation and anti fuse programming for connections. There are a number of hardware illustration languages. The principle characteristics of any language is to explain the purpose of a chunk and impartial to the structure of hardware. The common in use are: Verilog, VHDL, AHDL and ABEL.Verilog is presently a dominant language to describe hardware (Hardware Descriptive Languages). Investigating effectual picture transforming schemes to improve facts content material and to enhance the notion of in- motion articles is the focus of this work. It concentrates on visual heritage extraction and put into effect hardware framework for a chip like FPGA with collateral data computing to discover transferring articles in actual time subtraction of the heritage photograph. The capture of snap shots is hold on by a motion-picture camera with a proposition having $m \times n$ picture elements and a feed of q frames per second. It is related to an analog to digital converter where digital video information is computed in actual time in FPGA.In order to implement efficient hardware architecture for parallel data processing a methodology will be developed to realize the lay out. The technique of background subtraction will be used to further decrease the data processing complexity in order to minimize the power utilization for implementation of the above stated architecture. Finally required chip area can be reduced by using minimum numbers of registers, wires, LUT’s with the application of tools like Verilog and Mat lab.

Key words: FPGA, Look Up Table, Matlab, Verilog, Digital Image Processing, Background subtraction.

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1. INTRODUCTION

Moving objects may be diagnosed by detection structures that apply computer observation as the object moves in forefront of a digital photographic camera. The prime task is to obtain identification in absolute time, and to support in visible evaluation, a hard drive structure in Field Programmable Gate Arrays (FPGA) might be applied for video computing focused at the identification of moving items using the Backdrop subtraction method. In that case, some techniques are essential like digital photo processing, video subdivision and actual-time video computation. Aforementioned study is to look at digital photo processing, backdrop Subtraction methods and FPGA for the expansion of the structure in the case of video processing for the detection of in motion objects.

1.1 Digital Image Processing

The word "image" is related to the two range of light depth feature f (x, y), x and y are the dimensional coordinates and utility of f for any factor (x, y) is proportionate to the brilliance (or gray colour) for the picture at that factor, wherein x and y corresponds to the dimensional coordinates. Digital image accommodates hard drive, software and conceptual foundations; all convolute for obtaining the data of scrutiny monitored from a sequence. It is used as one of digital computing steps in the case of segmentation.

1.2 Video Segmentation

Video subdivision is a basic method in which the photo is partitioned into elements or component articles, equal to the extent wished for each application, that is, selection happens until the items of attraction are singled out from the picture vanguard. The items of interest mention to the institution of pixels those have a communal function in the photo. An illustration of item segmentation may be characterized with the aid of background subtraction method of photo, in which the initial few frameworks are encapsulated for production of the basic prototype with no item to be discovered and subsequently video input may be used to encapsulate new frames, known as the present frame. Within the categorization degree, the article is identified by reducing every one pixel in the present body from every one pixel of referred body. In the end, the resultant subtraction is subdivided photograph to spotlight areas of the photo movement.

1.3 FPGA (Field Programmable Gate Array)

The principle characteristic of FPGA chip is that it's far reprogramming and utilizes SRAM generation and anti fuse programming for connections. It is also being changeable and adjustable to every software. Chip can be laid-down through computer programme. It is defined as pretty concentrated positioning of little chunk of circuits. It includes flip-flops and a few logic gates with a few interfacing signals. So, we get the benefit that a solitary chip may consist of embedded complicated structures with high, medium and low extent of algorithms. The elementary composition in FPGA consists of three primary factors: connections, adaptive good judgment CLB blocks and I / O (input / output) blocks.

1.4 Background subtraction

It is a method in which photo's forefront is extricated for further computation (article recognition and many others). Normally picture's area of interest are articles (humans, vehicles, textual content etc.) in its forefront. Beside the degree of photo pre-processing article localisation is needed which might also employ this method. Backdrop subtraction is an extensively used proposition for the detection of in motion objects in films from stable cameras. In this technique, detection of the transferring articles from the distinction between the present frame and a referral frame, frequently called "background image", or "background model". Backdrop subtraction is mainly done when the photograph in query is a piece of a video streamlet. Backdrop subtraction presents principal cues for innumerable programs in computer perception, as an example supervision monitoring or humane poses evaluation.

1.5 Hardware Descriptive Language

There are a number of hardware illustration languages. The principle characteristic of that is to explain the purpose of a chunk and impartial to the software structure of hardware. The common in use are: Verilog, VHDL, AHDL and ABEL.Whereas Verilog is presently a dominant language to describe hardware (Hardware Descriptive Languages). Gateway Design Automation created this software in 1985 and subsequently Cadence Design System expanded it. It is described as IEEE standards 1364 and 1995. The Verilog concept tiers are distributed into behavioural, Port logic, Register Switch Degree (RTL) and layout. Every concept describes the depth of design detail for a specific illustration.

2. LITERATURE SURVEY

Piccardi (2006) proposed that Running Gaussian Average is one of the methods used to update the background model used for background subtraction. Updating the background model is an important part of background subtraction algorithm as it helps to incorporate various changes that occur in background over time due to change in illumination and other factors.

Cardells-Tormo and Molinet (2006) proposed that two dimensional (2-D) convolutions are similar to simultaneously figuring every pixel in the output image utilizing encompassing data i.e. a moving window of pixels. In spite of the fact that the operation is basic, the hardware is moulded in such a way that because of transmission capacity proficiency full raster lines must be perused from the outside memory. Furthermore, a line major image output ought to be performed to help shift-variant convolutions. While broadening the models created in earlier workmanship to help shift-variant convolutions; we understand that they require a lot of on-chip memory. While this reality may not have a substantial cost increment in ASIC executions, it makes FPGA executions costly or not feasible. Few novel FPGA-productive structures were proposed for producing a moving window over a column insightful print way. Since the proposed ideas have diverse throughput and asset utilization, they provide criteria to pick the ideal one for any outline point.

Zhu, Xia, Zang and Belloutia (2007) proposed that image slicing up is a key innovation in image transformation whereas threshold slicing up is some of the strategies utilized habitually. Usually a single threshold or a few threshold levels are chosen in conventional threshold dependent segmentation methodology; it is hard to extricate the multiplex data in a photo. Every pixel in a photo has its threshold set. For this type of calculation, the threshold value for a pixel in a particular image is assessed by computing the mean value in the case of the gray scale evaluations for its neighbour pixels. The difference in the square of the values of gray scale in the number of pixels of neighbour are likewise calculated as an extra judge state. The outcome of the proposed methodology is the edge of the image. Indeed the proposed methodology is equivalent to edge detection system for processing of an image. The proposed calculation could create exact image edge, while it is sensible to evaluate the threshold of a pixel through the measurable data of its neighbour pixels.

Ming (2010) proposed segmentation and genetic algorithm applications in picture segmentation. This paper proposes a few modifications for the conventional genetic algorithm and applies the enhanced genetic algorithm in picture segmentation. The enhanced genetic algorithm can stimulate the union while keeping up the populace at decent variety. Its strength is essentially superior to the fundamental genetic algorithm.

Mcloughlin and Bretschneider (2010) proposed that shuttle normally utilize uncommon and costly radiation tolerant, emission solidified or possibly military certified parts for calculations and other operation basic sub-systems. Reasons incorporate dependability in the brutal condition of room, and systems similarity or legacy with past operations. The superseding dependability treats the maximum satellite registering networks to be somewhat traditionalist in configuration. It also keeps away from novel or business off-the-rack parts. This paper portrays an option approach; a FPGA-mediated parallel architecture that enables unfit business gadgets to be consolidated into a computational gadget with total unwavering quality figures like those of customary space-qualified options. They give undeniable money saving advantages in moving to business off-the-rack gadgets, these are alluring in circumstances where to bring down power utilization as well as elevated processing execution are also needed. The final contention is especially of significance when the whole amongst required and accessible processing capacities for satellites are extending. An examination analyzes the suggested architecture for normal options to keep out the danger of inability inside demanded quantities and talks about vital implementations of the collateral architecture.

Kumar and Verma (2010) proposed that the value of the image pixels is converted from RGB to Grey using $Y=0.21\ R + 0.72\ G + 0.07\ B$.This is done in order to ease the computation. Now the design will only require computations on one channel compared to the three channels in the case of RGB color map. Thus the area of design can be reduced.

Chapman, Ranka and Majumdar (2011) proposed an outline for an effective system for recreating pictures given manufactured opening radar statistics utilizing the Unit for Graphics Processing i.e. (GPU). The plan, which is advanced to be utilized in GPU having a make of nVidia Tesla C2050, allotments the turnout picture into blocks. Specifically, our approach depends on the way that the measure of reaction statistics desired for processing each block is unsurprising and relative for the measure of the block partitioned by the span of the picture. Each string hinder with in GPU works

on single block for a provided arrangement of heartbeats out of the beat reaction framework. The ideal block measure is the biggest tile, with the end goal that a solitary heartbeat should be accommodated in GPU allocated memory, which still creates abundant strings to allow the system used for GPU to adequately make utilization only for 448 cores.

Ayinala, Brown and Parhi (2012) have displayed a novel way by which the FFT architectures are used to deal for a stated algorithm. The suggested methodology can be utilized to determine mostly collateral architectures of any subjective similarity amount. Utilizing this methodology collateral architecture has been recommended for the calculation of complicated FFT in light of radix-2 formulae. Utilization of power may be diminished up to 37% and half in suggested Two-Parallel architecture and Four-Parallel architecture in each individual case. These architectures show improvement for the situation where the inputs provided of real-esteemed category. In the case of RFFT, two diverse planning paths have been suggested. One having smaller complication in constraint rationale whereas alternate having less postpone components. Because of the ability of handling two information tests simultaneously, the recurrence of task may be lessened by two, thus diminishes utilization of power up to half. These techniques are extremely appropriate for administration in inbuilt or compact gadgets because of their little region and utilization of power. The authentic FFT configurations are not completely used. Efforts can be done in future so that FFT architectures will be coordinated for real-esteemed signs with complete equipment use.

Chenini, Derutin, Aufrere and Chapuis (2013) proposed an enhanced MPSoC way to deal with configuration, test, assess, and produce collateral analogous configurations which fulfil the extreme necessities in real-time picture handling implementations. In case of in stallions of multiprogramming executions productively, we connected our MPSoC type depiction and technique to build up a FPGA type multiple processing framework with various channel phases. This analogous outline goes for adjusting the calculation necessity and sufficiently giving registering exhibitions to guarantee real time handling of complicated picture/video preparing theorems. Our principle target is to empower snappy executions in FPGA by building up another structure that goes for creating an ideal MPSoC in a particular application. The client has just to configuration picture/video handling implementations in language C and change over the system hardware utilizing Cube- Gen device.

Darji, Kushwah, Merchant and Chandorkar (2014) proposed superior RMA, PMA and FMA with double-pixel filtering strategy for figuring multi-stage 2-D DWT. The designs are thought about based on assets used and swiftness. Miniature-channeling is utilized in foresee/refresh processor component to decrease the basic way. The proposed FMA in the case of lifting (5, 3) and lifting (9, 7) utilizes just 2N line and 4N line cushions, individually. The suggested PMA is straightforward, general and measured. It can be fell for n-stage deterioration. In addition, it requires just 4.8 N line supports for five-level deterioration, subsequently lessens line cradle around half than other comparative outlines. The suggested RMA utilizes sixteen multipliers along with twenty four adders in the case of n-level disintegration. Besides, a necessity of line cushions is autonomous in the level for disintegration. The suggested configurations are executed on Xilinx software while using FPGA of Virtex type. When the suggested plan is executed on FPGA, it demonstrates better frequency response, lesser latency, and low power consumption when contrasted with different architectures with similar particulars.

Tabkhi,Sabbagh and Schirner (2014) proposed a method that quickly portrays an acknowledgment based on FPGA in regard with the MoG background subtraction that is working for full- High Definition framework resolution. Their Hardware hand-created MoG comprises of seventy seven pipeline phases working at a frequency of 148.5 Mega Hertz actualized on a platform of Zynq-7000 System on Chip. This gives better productivity and the power utilization goes less than 500 milli Watts.This mechanism is 600 times more effective as compared to an implanted software arrangement.

Cherian,Singh and Manikandan (2014) proposed that Background subtraction is one of the strategies utilized as a part of video observation framework for distinguishing moving objects in a video. The author proposed a background subtraction strategy which gives result notwithstanding while camera is not stable. There are many difficulties that need to be considered for building up a strong background subtraction technique majorly brightening changes. The input frames are correlated and amend according to source frame at that point isolating the frontal article with regard to backdrop. Background subtraction may be made extremely productive in the case of FPGA device that should produce 640x480 video arrangement. Test outcome demonstrates that it can distinguish the moving article quickly. It can unravel different issues like complex

calculation, transmission of information, hardware assets cost and so forth. The continuous video was caught by utilizing Vmod CAM.

Pagire and Kulkarni (2014) proposed that Background Subtraction technically involves extracting the moving foreground from the static background. This is easy if we have an image of the background alone. Then we would just need to subtract the background image from the current image. This is known as a static background model. But in most cases, we need to extract the background from the images. This becomes difficult when we have varying illumination or shadows in the images. Since the shadow is also moving, a static background model is not sufficient and we require a dynamic background model

Hatwar and Bichwe (2015) proposed that Cognitive Radio should be a standout amongst the most astute radio if it is designed powerfully. The transceiver is composed with the end goal to utilize the maximum wireless channels. Cognitive Radio utilizes plain spectrum facility very smartly according variation in the conditions. It has the ability to modify the radio specifications. Hence the radio consequently identifies accessible channels for wireless condition. At that point as need amends its channel level specifications to permit many proficient wireless interchanges for a particular range band in single area. Main concentration of the work carried out is to limit defer furthermore expanding throughput of controlling engine. This paper also demonstrates the programming prototype configuration and one of the utilization of Genetic Algorithm operated Field Programmable Gate Array type basic controlling engine in Cognitive Radio was displayed.

Jahiruzzaman, Saha and Hawlader (2015) suggested that 2D Convolution technique is the best helpful to investigate digital photo and processing of video and has an assortment for processing digital image. It has applications like image enhancement, edge detection, photo segmentation, obscuring and smoothing. A photo is connected for processing of video on the premise using frame by frame for movement identification. Despite the fact that the computing complication in 2D convolution is very high because it requires high state parallelism for item and addition functions. However it can have applications for real time embedded framework like a full custom ASIC or FPGA. Convolved image straight forwardly relies upon the kernel and proposed design is reasonable in the case of kernel having 3x3magnitude. Implementation and synthesis of FPGA based image processing framework for 2D convolution was performed. This design was simulated using Verilog and FPGA of Virtex-5 series for synthesis. The outcome demonstrates that the

suggested architecture utilizes lesser quantity of blocks (LUTs and registers) as compared to other types of designs. It also has less amount of time delay. Since the intricacy of the suggested design is less therefore it may be used as a part of image processing applications.

Mervin and Sarala (2015) proposed that optical prostheses administers electrical stimulation in the various components of the optical pathway. It has been put forward as a feasible way to deal with re-establish practical vision. This perception is right now constrained because the small resolution photos belong to a predetermined numeral of simulating electrodes. On these lines, techniques to enhance the visual statutes giving helpful visual data are to be considered. The systems meant for processing of Image depends on a novel background subtraction procedure to improve the substance of dynamic scenes of everyday life. It was demonstrated that background decrease or background diminishment with closer view upgrade, expanded reaction precision that specifically combined pixels to lesser resolution. If more dim scale data is included then a background decrease/frontal area increment procedure brought about the best execution. It also provides the most elevated acknowledgment exactness. Advance improvement in the constituents of image - processing for optical prostheses depends on certain outcomes. It will help embedded beneficiaries to maintain a strategic distance from risky circumstances and accomplish free versatility in today's life.

Bourrasset, Maggiani, Serot and Berry (2015) suggested that Optical flow technique involves calculating the optical flow of the image and performing clustering based on the optical flow distribution. The large amount of calculations and its poor anti-noise performance are the reasons for making it unsuitable for real-time conditions.

Prabhu. et al., (2016) proposed that with the high demands of sequencing in the area of technological research, it is required to develop speedy sequencing process. Smith Waterman methodology is used for one of the main sequencing operation. This methodology is in use for two traditional paths to estimate the components of matrix. These are (a) Sequential processes (b) Conventional parallel processes. Consider these both of these phenomenons and develop a new method. Because of three methods by two main goals are met i.e. (i) smaller time for the calculating matrix components (ii) optimization of processor being used. Although later one is conventional but parallel processing $\{(2m)\}$ is speedy as compared with sequential processing (mn). This work made an effort for reduction of timing to a scale of (m) by Cross Diagonal

Element Wise Parallel Processing Approach (CDEWPPA). Optimization of processor for the conventional parallel and CDEWPPA is finished with a adequate result.CDEWPPA functions better as compared to the traditional parallel methodology for query implementation time test and for speed up ratio also.

Jarrah (2016) proposed that Kalman filter has been turned out to be an extremely powerful strategy to identify targets in a proficient and exact way. It gives productive estimations when the precise nature of the modeled system is obscure in the presence of estimation and process noise. Notwithstanding, Kalman filter is computationally broad particularly in Multi Target Tracking (MTT) radar system. Along these lines, it is alluring to apply it on advanced parallel architecture for example, FPGA, GPU, and multi-cores to increase performance and accomplish continuous prerequisites. In this paper, the author displays a productive parallel architecture of Kalman filter on various stages, for example, FPGA, GPU, and multicore. Kalman filter operations are done on a single core CPU before they are decomposed, parallelized, planned, and mapped into FPGA and GPU stages. The test demonstrate the suitability of utilizing FPGA and GPU stages to perform single processing in real time. Parallel architectures can altogether outflank an identical successive execution due to their pipelined architecture, custom usefulness of VLSI ASIC gadgets, adaptability, and flexibility. Their simulation results demonstrate that the achieved speed-up of FPGA and GPU over the successive one is enhanced by up to 37.76 and 31.93, separately.

Save and Jadhav (2016) proposed that high requests for standard of component and profitability drives industry to utilize automatic recognition system. High momentum deformity detection strategy is desirable for manual investigation. The work suggested a strategy for recognizing deformity on roller exterior utilizing FPGA chip. A methodology is presented for identification of imperfection in roller photos with effective hardware design along these lines actualizing genuine time implementation in mechanical production. The devoted engineering is intended for roller imperfection identification on FPGA. Laplace edge detector is utilized in high pass filters to obtain improved edge detected photo which is divided additionally to identify the imperfections. The results show that the judgement of imperfection identification is enhanced along with better precision. The suggested calculation demands sixty milliseconds for imperfection recognition with its area.

2.1 Gaps in Literature

Large amount of data to be processed in object detection takes time if processed serially, which is not suitable for real time environment. The parallel processing capabilities of FPGA help resolve this issue. Moving object detection is associated with problems like illumination variations, poor video quality leading to noise and dynamic background. While discussing the references, it is observed that there has been little work in the architectures for parallel data processing in specifying or detailing the importance these problems. Designing of robust algorithm for object detection using background subtraction is required to be explored in detail for the solution of these problems which is also going to reduce the required chip area in FPGA by using minimum numbers of registers, wires and LUT's.Modifications in the existing parallel architectures are to be looked into so as to provide better performance and achieve high precision. The techniques researched must be reliable, very highly efficient and real-time in the case of moving objects identification. The issue of power utilization in implanted software is to be investigated deeply for minimum power consumption so as to have a value of few milli Watts in MoG background subtraction when implemented on FPGA for successful practical and real time applications.

3. DESCRIPTION OF BROAD AREA

Image splitting up is the method of subdividing a digital image into numerous segments (components of pixels known as top notch pixels). The reason of splitting up is to make easy the changes in illustration of a photograph which are significant. It is easier to analyze but this turns into a hard challenge while it needs to be expanded in real time. It also requires the computing of considerable quantity of facts and commands. Consider a picture having a proposition of $m \times n$, eight-bit quantisation, q frames consistent with 2d and 3 shade constituent (RGB).It would procedure p Mega bytes in a second while the computation does not get always finished in real time. The photo can have available traces according to the motion of humans. It has low resolution because of the decrease in the aggregate of computed pixels

Psychophysical consequences showed that historical past subtraction or history discount with fore front augmenting, improved response reliability as equated with techniques that at once consolidated pixels to decrease decision. Through adjoining greater gray scale facts, a heritage

discount/forefront improvement strategy emerged within the optimum implementation and top level reputation reliability. Similarly improvement of picture computing calibre for a optical prosthesis established totally on those effects will help installed beneficiary to keep away from threatening conditions and reap individualistic movability in everyday lifestyles.

Fundamental downside of Background subtraction is shadow which is classified as a part of foreground. This is because shadow share identical movement styles as that of foreground. This brings about fake detection of foreground objects which decreases the overall performance of the object monitored. Consider scenarios wherein detection and monitoring overall performance are affected firstly because of shadow, near items gets merged collectively and secondly because the shadow pixels are detected they decrease the reliability of the advent version for everyone, increasing the probability of monitoring loss. There are forms of shadows especially, that part of the object which is not illuminated is referred to as self-shadow and the region projected at the scene by the item is known as cast shadow. This last one is more nicely known as transferring forged shadow if the object is transferring.

Investigating effectual picture transforming schemes to improve facts content material and to enhance the notion of in motion articles is focussed right here. This work concentrates on visual heritage extraction and put into effect hardware framework for a chip like FPGA with collateral data computing to discover transferring articles in actual time subtraction of the heritage photograph. The capture of snap shots is hold on by a motion-picture camera with a proposition having $m \times n$ picture elements and a feed of q frames per second. It is related to an analog to digital converter where digital video information is computed in actual time in FPGA.In our case m, n, p *and q* are the parameters which are dependent on the hardware configuration of FPGA.

4. OBJECTIVES OF STUDY

4.1Problem formulation

To improve the current architectures, there are numerous possibilities for future in the case of item segmentation and the object monitoring. Irregularities can be removed due to sudden mutations in background image so as to reduce the tailing effect in objects that moves very quickly and the cavities appear along with a low momentum. FPGA based object tracking system and accelerated abandoned object detection can be designed using modified architectures which are

having practical applications. The power and area efficient architectures can be designed using FPGA so as to overcome the various gaps discussed in literature survey for video sequence having resolution like 800x600, 640x480, 320x240 or 144x180 which produces several Megabytes of parallel data.

4.2 Objectives

The following shall be the objectives of proposed research.

1. To go through related literature and conceptual understanding of problem statement

2. To realize hardware efficient lay out for collateral data computing.

3. To further decrease the data processing complexity by incorporating the technique of background subtraction.

4. To reduce required chip area for the model by using minimum numbers of registers, wires and LUT's.

5. To minimise the power utilisation to implement the above stated architectures.

5. METHODOLOGY TO BE ADOPTED

Details of proposed methodology, work flow and tools have been mentioned below**.**

5.1 Phase-I

The basic method is video segmentation where the photo is spilt up into parts or component articles for a particular level according to usage. This process is continued for the isolation articles of interest from the photo forefront of belonging to the reference image. The successfulness or non-success for the analysis is controlled by the method. Division of the video into frames is done using MATLAB.

5.2 Phase-II

The design contains photo acquisition, choice of the value for the threshold for every color constituent of the photo, segregating the constituent Y, Cb & Cr of the color, statistical computation using the photo gray levels, calculations of the difference in the mean image and the

present image for Y, Cb & Cr in each color constituent providing pixel to pixel differentiation for every components.The thresholds are of three types namely threshold uses low values, balanced threshold values and threshold uses high value. Deciding the threshold value of different colour components is very important and done precisely.

5.3 Phase-III

The classifications of image elements for the objects or the backdrop image are used for the comparison after determining the threshold value. The replacement for photo elements for their similar values from the test article image will be performed for every color component, but the pixels belonging to the background color does not cause replacement. Background subtraction is done to eliminate non- participating elements of image.

5.4 Phase-IV

The recognition and detection of articles in a frame is a key factor for video segmentation. Main function is to subdivide the photo into its integral elements. The procedure is carried out till the objects of interest are obscured from application point of view. A bunch of pixels having common characteristics are known as objects of interest.

5.5 Phase-V

MATLAB software will be used for designing the algorithm for the Fixed Point and Floating Point method. These are two kinds of approaches for generating the data base of images. A number of threshold values are chosen for making the comparisons of the parameters for both methods in order to evaluate the detection of objects. This result decides the implementation of a particular method for the data base of the photo.

5.6 Phase-VI

The proposed architecture is going to be modelled using Verilog which is hardware descriptive language. Xilinx Vivado design suite will be used as simulation and synthesis tool for loading the frames into FPGA memory

5.7 Phase-VII

RTL design is to be done in Verilog for every module for background subtraction and object detection. It provides the time-related information which is restricted to records, clock cycle, and logic in the group of them is set. We do not get information about the technology and know about existing architecture only.

5.8 Phase-VII

Analysis of various hardware specifications like Slice Registers, Slice LUTs, Block RAM, DSP Blocks and IOBs of FPGA will be done in terms of utilization and availability.

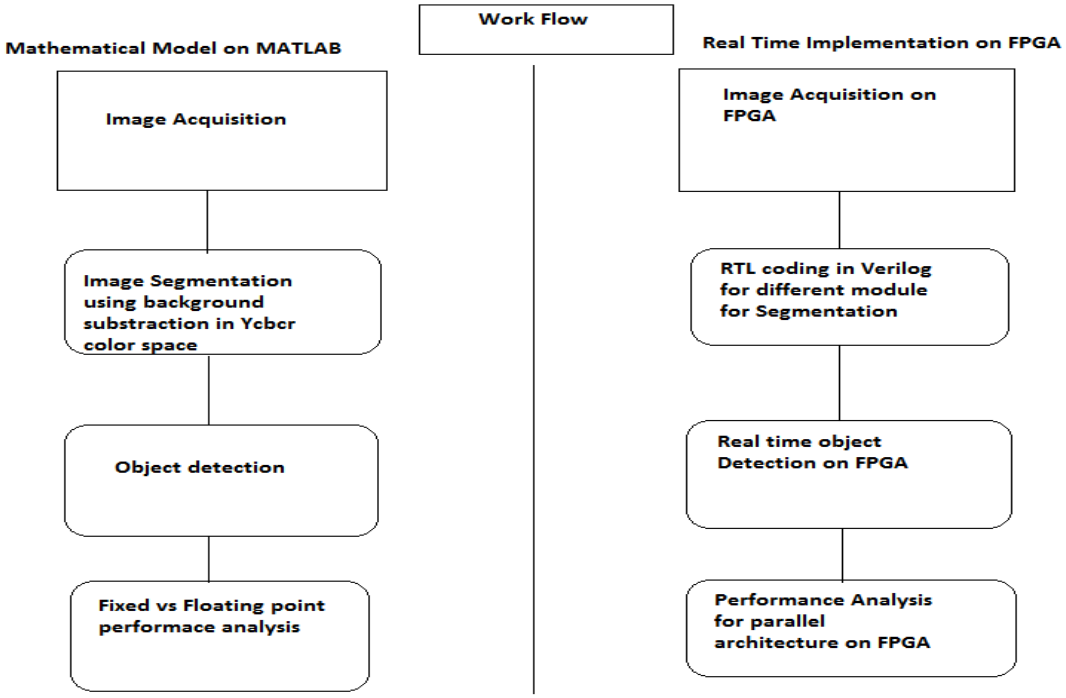
Work Flow
Mathematical Model on MATLAB
Image Acquisition
Image Segmentation using background substraction in Ycbcr color space
Object detection
Fixed vs Floating point performace analysis
Real Time Implementation on FPGA
Image Acquisition on FPGA
RTL coding in Verilog for different module for Segmentation
Real time object Detection on FPGA
Performance Analysis for parallel architecture on FPGA

Fig. (1) Design flow of FPGA hardware architecture for parallel data processing

6. EXPECTED OUTCOME OF RESEARCH

During the study of the performance analysis of fixed point v/s floating point for object detection low threshold parameters may result for every component in the identification of numerous false

positives, balanced threshold parameters may result in the identification of numerous true positives and high parameters may result in the identification of numerous false negatives. A modified architecture may be proposed for the detection of moving object. Comparison of conventional and proposed techniques for different number of frames per second configurations will be done and it is expected that increment in number of frames per second will give better results in terms of object detection. Implementation of background subtraction technique for dynamic model will be done which will require minimum of area on FPGA for various spaces like Slice Registers, Slice LUTs, Block RAM and DSP Blocks. Total on-chip system power consumption of our design will have minimum value in the range of few mW when implementation of proposed model is performed on FPGA.

7. Proposed Time Frame

Time Frame	Dec. 16 June 2017			July-Dec. 2017			Jan.-June 2018			July-Dec. 2018			Jan.-June 2019			July-Dec. 2019			Jan.-June 2020			July-Dec. 2020		
Months	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34		36	38	40	42	44	48
Year	1						2						3						4					
Course Work																								
Literature Survey																								
Review paper based on Literature Survey																								
Base paper Implementation for achieving objective 1																								
Objective 2																								
Objective 3																								
Objective 4																								
Objective 5																								
Miscellaneous works																								

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